NeoLoch

Inquisitor 4116 DRAM Blade Manual

Overview

The Inquisitor 4116 DRAM blade is designed to test 16 pin DRAM ICs. Current tests include 4116, 9016, D416, 402, 4096 and UPD414 (V2 firmware only). The Inquisitor 4116 DRAM tester can conduct fast two pass test or a more in depth test to discover if a DRAM is good or bad.

April 2017

This document details the operation of the default configuration of the IC tester as well as details on the device's operation for custom code design.

Information contained in this document is provided for your convenience only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. NeoLoch makes no representations or warranties of any kind, expressed or implied, related to the information contained in this document. NeoLoch disclaims all liability arising from the information contained in this document and its use. Use of NeoLoch devices in life support and/or safety applications is entirely at the buyer's risk. And, the buyer agrees to indemnify and hold harmless NeoLoch from any and all damages, claims, suits, or expenses resulting from such use.

Trademarks
The NeoLoch name, the NeoLoch logo, and Fireloch are trademarks of NeoLoch, LLC in the U.S.A.

Table of Contents

1.0 Device Connection & Power Requirements

1.1   CN1 – Card Edge Connector

Edge of PC board that plugs into the card edge socket on the Inquisitor Core PC board. When plugging in the SRAM Blade, line up the white triangle with the white triangle on the Core PC board.

1.2   CN2 – ICSP (In-Circuit Serial Programming)

ICSP connector, this port is designed to attach to a PICKit 3 or compatible programmer.

1.3   LED 1 – Power LED

Indicates when power is applied to the Blade.

1.4   Power Requirements

	Minimum	Typical	Maximum
VCC	4.5V	5.0V	5.5V
VDD	10.8V	12.0V	13.2V
VBB	-4.5V	-5.0V	-5.5V

Make sure the +12V side is using a regulated source. These DRAM ICs use the +12V supply as part of their power scheme. The -5V is supplied via the TC7662 voltage inverter and will be the opposite of the +5V supply.

2.0 Understanding the DRAM Testing Process

To begin testing a DRAM, use the following steps:

- Insert the DRAM blade into the Core module.
- Power up the tester.
- Insert the DRAM IC to be tested into the ZIF socket, make sure pin 1 is the closest pin to the ZIF's lever.
- Lower the lever to lock the DRAM in place.
- Press the left or right arrow key to select either the 4116 / 9016 / D416, 4027 / 4096, or the UPD414 test.
- Press the enter key to start the test.

2.1 Menu System

Pressing the ← or → keys will guide your through the menu system, which consists of:

2.1.1 – 4116 / 9016 / D416

Test 4116 DRAM and compatible DRAM.

2.1.2 – 4027 / 4096

Test 4027 DRAM and compatible DRAM.

2.1.3 – Long Test

Note: Available on the 4116, 9016 and D416 DRAM only.

Determines if a long or short test is done when testing DRAM, yes = long test and no = short test.

Short Test: The DRAM is written with all zero's and then all one's. This is a quick test but may not discover all problems with a bad DRAM, this test consists of:
Note: as of firmware verions 2.1, the short test is no longer available on the 4027, 4096 and UPD414 tests.

Scan 1: Writes all zeroes to the DRAM and then reads the data back for comparison.
Scan 2: Writes all ones to the DRAM and then reads the data back for comparison.

Long Test: The long test does a far more extensive investigation of the DRAM and will discover problems the short test will miss. This test consists of:

Scan 1: Writes all zeroes to the DRAM and then reads the data back for comparison.

Scan 2: Writes all ones to the DRAM and then reads the data back for comparison.

Scan 3 – 18: The long test is a far more intensive look at the DRAM's capability to store, retain, and retrieve data correctly. The idea behind this test is to write a wide variety of changing data to each and every address. To accomplish this in a timely manner the following scheme is used:

First, the DRAM's memory is divided up into 8 bit chunks (bytes).

Two counters are used to generate values for the upper and lower nibbles. Counter 1 decrements and counter 2 increments. The low nibble of counter 1 is placed in the current DRAM's address range upper nibble, and the lower nibble of counter 2 is placed in the lower nibble. So:

DRAM bits 7 – 4 = Counter 1's lower four bits (lower nibble).
DRAM bits 3 – 0 = Counter 2's lower four bits (lower nibble).

So, if counter 1 & 2 both = 0 and we are on the very first byte range in the DRAM's memory, then bits 0 through 7 DRAM would all be clear. Byte 0 (address's 0 through 7) = 0x00.

Next, counter 1 is decremented, so would equal 0xFF. Counter 2 is incremented and equals 0x01. The following table illustrates this process and how the data changes for each byte in the DRAM over each scan.

	Scan 3	Scan 4	Scan 5	Scan 6	Scan 7	Scan 8	Scan 9	...
Bits 0-7 (Byte 0)	0xF1	0xE2	0xD3	0xC4	0xB5	0xA6	0x97	...
Bits 8-15 (Byte 1)	0xE2	0xD3	0xC4	0xB5	0xA6	0x97	0x88	...
Bits 16-23 (Byte 2)	0xD3	0xC4	0xB5	0xA6	0x97	0x88	0x79	...
Bits 24 -31 (Byte 3)	0xC4	0xB5	0xA6	0x97	0x88	0x79	0x6A	...
Bits 32 -39 (Byte 4)	0xB5	0xA6	0x97	0x88	0x79	0x6A	0x5B	...
Bits 40 -47 (Byte 5)	0xA6	0x97	0x88	0x79	0x6A	0x5B	0x4C	...
Bits 48 -55 (Byte 6)	0x97	0x88	0x79	0x6A	0x5B	0x4C	0x3D	...
...	...	...	...	...	...	...	...	...

For 4116 DRAM the long test takes approximately 28 seconds.
For 4027 DRAM the long test takes approximately 10 seconds.

2.1.4 – Statistics

V2 code added the statistics recording. To access statistics first press the left or right arrow key to clear the bad ram detect flag and then return to the test you wish to see statistics for. The press the down arrow key, statistics will be displayed which included the total number of tests, how many passed and how many failed. This menu item will only be displayed when the bad ram flag is clear.

2.1.5 – Multiple Scans Per Test

V2 code added the ability to do multiple scans each time you press the enter key. To access this feature first make sure the bad ram flag is clear, you can do this by pressing the left or right arrow key and then returning to the test you wish to modify. Next, press the down arrow key twice or the up arrow key once. You can change the setting using the following keys:

- Left Arrow: add 10 to the test total.
- Right Arrow: add 1 to the test total.
- Enter: Reset test total to 1.
- Up and Down: Move to next setting / return to test main menu.

Each test has it's own statistics and multiple scan setting.

Example: If you change the number of scans to 10 and then test a RAM, the test will be run 10 times on that RAM. This allows you to test a RAM multiple times without having to keep pressing the enter key for each test.

2.2 LED Result

At the conclusion of a test, LED 3 on the main board will visually display the result. Green means the DRAM passed and red means the DRAM failed. During the test the LED will be orange.

2.3 Display DRAM Results.

If a DRAM tests bad, you can use the up and down arrows keys to get a better idea of what happened during each scan. The first address a bad bit was detected at is listed along with the number of bad bits encountered during that pass.

3.0 Schematic

4.0 Card Edge to MCU Connections

Below is a table that lays out the pin assignment between the card edge connector, the MCU and the Port Expander.

Card Pin #	Function	Card Pin #	Function
2	+5V	1	+12V
4	Ground	3	Ground
6	Card Error LED (Gnd to turn LED off)	5	Not Connected
8	ZIF Pin 1 – VBB -5V	7	ZIF Pin 40 – GND
10	ZIF Pin 2 – MCU RA1	9	ZIF Pin 39 – MCU RB6 (PGC)
12	ZIF Pin 3 – MCU RA2	11	ZIF Pin 38 – MCU RB4
14	ZIF Pin 4 – MCU RA3	13	ZIF Pin 37 – MCU RB3
16	ZIF Pin 5 – MCU RA4	15	ZIF Pin 36 – MCU RA6
18	ZIF Pin 6 – MCU RA5	17	ZIF Pin 35 – MCU RB1
20	ZIF Pin 7 – MCU RA7	19	ZIF Pin 34 – MCU RB0
22	ZIF Pin 8 – VDD +12V	21	ZIF Pin 33 – VCC +5V
24	ZIF Pin 9 – NC	23	ZIF Pin 32 – NC
26	ZIF Pin 10 – NC	25	ZIF Pin 31 – NC
28	ZIF Pin 11 – NC	27	ZIF Pin 30 – NC
30	ZIF Pin 12 – NC	29	ZIF Pin 29 – NC
32	ZIF Pin 13 – NC	31	ZIF Pin 28 – NC
34	ZIF Pin 14 – NC	33	ZIF Pin 27 – NC
36	ZIF Pin 15 – NC	35	ZIF Pin 26 – NC
38	ZIF Pin 16 – NC	37	ZIF Pin 25 – NC
40	ZIF Pin 17 – NC	39	ZIF Pin 24 – NC
42	ZIF Pin 18 – NC	41	ZIF Pin 23 – NC
44	ZIF Pin 19 – NC	43	ZIF Pin 22 – NC
46	ZIF Pin 20 – NC	45	ZIF Pin 21 – NC
48	Switches – MCU RB5	47	I2C – SCL – MCU RC3
50	Not Connected	49	I2C - SDA – MCU RC4

5.0 Parts List

- 1 – Printed circuit board
- 1 – 40 pin socket
- 1 – 8 pin socket
- 1 – PIC16F1719 microcontroller (Programmed)
- 1 – TC7662 Voltage Inverter.
- 3 – Reed Relays (Polarized)
- 1 – 390 Ohm Resistor (Orange, White, Brown)
- 1 – 2x5 rectangle green LED
- 5 – 0.1uF Ceramic Capacitors
- 2 – 10uF capacitor

6.0 Firmware Versions and Known Bugs

Just like any other product, a number of issues have been discovered in the 4116 blade that effect testing. Fortunately there are ways around these problems. However, some of these issues are severe and NeoLoch is offering to upgrade all MCU's to the current firmware version at no charge, all you need to do is send in your current Microcontroller, we'll reprogram it (or replace if it's an older PIC16F1519) and mail it back to you. Please contact us if for mailing instructions.

A list of the various firmware versions is listed below:

6.1   V1.x MCU Firmware

1. Bad DRAM would fail on the short test, but pass on the long test. This is due to the error flag being cleared in between pass 2 and pass 3 and would only show up on DRAM that failed pass 1 or 2, but passed the remaining. To get around this, always test DRAM using both long and short tests to detect problems. V2 code corrected this issue for all tests.

6.2   V2.0 MCU Firmware

The 4027, 4096 and UPD414 DRAM reported inconsistent results when testing multiple scans or when pressing the enter key to start a new test immediately after a scan had finished. It is believed this is due to a residual charge present inside the test subject that is not allowing the DRAM to fully power down, please allow 5 seconds in between tests (pressing enter) and don't use the multiple scan option on the 4027, 4096, and UPD414. This problem doesn't appear to effect 4116 DRAM.

6.3   V2.1 MCU Firmware

V2.1 takes steps to correct the residual charge issue.

1. Due to the inconsistent results caused by the residual charge, support for the short test has been removed from the 4027, 4096 and UPD414 tests. The short test is still available for the 4116 test.

2. For multiple scans, the DRAM is being left powered through the entire process, eliminating issues caused by power cycling the test subject.

7.0 Cross Reference Chart

The following cross reference chart is intended to help guide you in determining if a specific DRAM may be testable using the 4116 blade. NeoLoch has not tested all the listed RAM and certainly not all the variants for each part number, and makes no guarantee that all variants are testable.

Manufacturer / Test	4116 / 9016 / D416	4027 / 4096 / UPD414
AMD	AM9016	
FAIRCHILD	F4116	
FUJITSU	MB8116	
MOSTEK	MK4116	MK4027 MK4096 MK4200 MK4227
MOTOROLA	MCM4116	MCM4027 MCM4096 MCM6604
NEC	UPD416	UPD414
NSC	MM5290	
OKI	MSM3716	
SIGNETICS		2660
TI	TMS4116	
TOSHIBA	TMM416	

Appendix A: Firmware Revision History

Firmware Version 1.0
- Initial Release

Firmware Version 2.0
- Fixed bad ram flag in between pass 2 and pass 3 that would pass bad RAM.
- Added support for UPD414.

Firmware Version 2.1
- Changed the code to leave the DRAM powered in between bulk scans.
- Removed short test on 4027, 4096 and UPD414 due to inconsistent results.
- Added a s mall delay on the short test between test 2 and the start of the next scan so that the results of test 2 are visible for a short period of time.

Appendix B: Document Revision History

Revision A (4/2016)
- Initial release of this document

Revision B (4/2017)
- Added "Firmware Version and Known Bugs" section.
- Added instructions on "Statistics" and "Multiple Scans" options.
- Added cross reference chart.
- Updated information on each firmware version.