NeoLoch

Inquisitor Static RAM 1 Blade V3 Manual

Overview

The Inquisitor SRAM blade works in conjunction with the Inquisitor Core Module and allows the testing of a wide range of static RAM types, including but not limited to:

- 2101 / 5101
- 2016 / 2018
- 2114 / 6514 / 9114 (also tests: TC5514 & 9914)
- 2125
- 2147
- 2148 / 2149
- 2465 / 6264
- 4016 / 6116
- 6810
- 7489 (Adapter Required for version 1.xx MCUs only.)
- 74189
- M5M5189
- 62256 / W24257
- W24512

This document details the operation of the default configuration of the IC tester as well as details on the device's operation for custom code design.

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1.0 Device Connection & Settings

1.1 CN1 – Card Edge Connector

Edge of PC board that plugs into the card edge socket on the Inquisitor Core PC board. When plugging in the SRAM Blade, line up the white triangle with the white triangle on the Core PC board.

1.2 CN2 – ICSP (In-Circuit Serial Programming)

ICSP connector, this port is designed to attach to a PICKit 2, PICkit 3 or compatible programmer.

1.3 LED 1 – Power LED

Indicates when power is applied to the Blade.

1.4 Bi-Color LED Setting

Use the left or right arrow keys to change the test to the LED setting. This setting allows you to swap the bi-color LEDs operation in case the LED was installed backwards. In essence, when this setting is reversed, the LED will operate in reverse to normal operation.

To change the setting, move to the LED setting and press the the "enter" key, the setting is stored in the microcontrollers internal flash memory.

1.5 Individual Test Statistics

To access statistics, select any test and press the down arrow key. The test name along with the total number of tests conducted, how many were good and how many were bad will be displayed. Pressing "enter" will bring up a prompt to reset the data, you can reset the data at this point with another press of the "enter" key or abort the reset by pressing the up or down arrow keys.

1.6 Multiple Test Setting

To access this setting, select the test and the ether press the up or down arrow keys until the "Scans Per Test" setting appears. To change the setting use the following keys:

- Left "<" = increase number by 10.
- Right ">" = increase number by 1.
- "Enter" = reset number to 1.

Changing this number will change the way a test works, instead of going through the full test just once, the test will include multiple overall tests. So, for example, changing this setting to 11 would test the RAM IC 11 times with a single press of the enter key. Each RAM test has it's own setting.

2.0 Understanding RAM Tester Scans

The tester was designed to be quickly and easily operated. RAM ICs can be inserted into the device while it is powered. When not testing, the ZIF socket is not powered and all pins are either at ground potential or in a high-impedance state.

2.1 4 - 8 Bit - Scans 1 through 16 – Memory Check

These scan consist of writing 0X00 through 0X0F for 4 bit memories, or 0X00 through 0XFF for 8 bit memories.

Scan 1 consists of writing 0X00 to each memory location and then reading the data back for verification. Each next scan will increment the test value by 0X01 (4 bit) or 0X11 (8 bit). This quickly covers all possible combinations and will bring out any flaws.

At the end of each scan a summary will be displayed on the LCD screen for higher memory devices. Lower memory devices test in just a few seconds, so no information is displayed for them at this point. However, this information can be displayed at the end of a test for those RAM ICs that fail.

2.2 4 - 8 Bit Pass 17 – Address Check

It's possible that a RAM IC's memory is just find while the addressing block has a failure, permitting, for example, two different addresses to access the same memory location. Pass 17 writes a different offset value to each memory location to detect if there's an address issue.

For 4-bit devices this consists of writing 0X00 to address 0X00, 0X01 to address 0X01, and so on. Once the program reaches address 0X10 however, the offset value kicks in and we write 0X01 to address 0X10. This offset value slowly increases with every rollover of the nibble that's being written to the RAM IC.

This offset will cause a bad address to come out on the read back, and reveal an otherwise hard to detect issue.

For 8 bit devices, the process is the same except the offset doesn't kick in until a rollover has happened from the full 8 data bits (byte).

2.4 1 Bit Pass 1 – Write and Read all 0's

During this scan, 0 is written to and read from each address.

2.5 1 Bit Pass 2 – Write and Read all 1's

During this scan, 1 is written to and read from each address.

2.6 1 Bit Pass 3 – Byte Read Write

This scan breaks up the RAM into as many bytes (8 bits) as the size of the RAM will permit, so addresses 0 through 7 becomes the first byte, 8 through 15 the second, 16 through 23 the third, and so on.

Each byte is then subjected to being written to and read from beginning with 0. After each read, the value being written / read is incremented by 1, this process continues until all 256 possible combinations have been written / read from the byte being tested.

During this test, the current range of addresses being tested will be displayed on the LCD screen.

2.7 LED Result

At the conclusion of a test, LED 3 on the main board will visually display the result. Green means the RAM passed and red means the RAM failed. During the test the LED will be orange.

When changing tests the result LED will be turned off.

2.8 Display Bad RAM Results.

If a RAM IC tests bad, the collected data on each scan can be displayed by pressing the up and down arrow keys on the right side of the LCD display. The first line consists of the scan number, the first address where a bad read was detected, and if the scan failed or passed. An example of what line 1 appears like: "S01 FBA:xxx FAIL or PASS"

Line 2 consists of the number of bad reads from that scan and a accumulation of the bad bits found in the scan. Good or not relevant bits are displayed with a "-", while bad bits are displayed with a "X". An example of this line: "L:FF B:----X--X"

3.0 Testing RAM Instructions

Before you begin testing an integrated circuit, there are some basic steps you can take to insure a good test result, they are:

1) It's important to note that any dirt or corrosion on the pins of the IC to be tested will cause connection failure between the IC and the ZIF socket. And, in turn this connection issue will cause the IC to fail all or parts of the testing process. To prevent this make sure the pins are clean and free of dirt and corrosion.

2) The IC needs to be seated in the ZIF socket correctly before being locked in place. The IC should sit flatly on the ZIF sockets surface with the pins inside the ZIF socket. Hold the IC in place with slight pressure while you lower the lever to lock the IC in place, this prevents the IC from lifting up while being locked.

To begin testing RAM

Step 1: Make sure the power is off, insert the SRAM blade and then turn the power on

Step 2: Use the left or right arrow keys to select the appropriate RAM test.

Step 3. Insert the RAM IC into the ZIF socket so that pin 1 is the closest pin to the ZIF lever, lower the lever, and then press the "TEST" key.

Troubleshooting failed ICs

If the IC under test fails take a look at the pins and make sure they are clean, not bent, or have any other obvious problems. Connection failures can be caused by dirty pins, incorrect seating in the ZIF socket, or the IC really is bad. Here are some steps to help determine the cause:

1) Raise the ZIF lever and shift the IC slightly and then lower the lever back down. Just moving an IC can resolve a test fail.

2) Look for bent or damaged pins, correct any issue and try testing again.

3) It's possible the connectors on the blade (called fingers) are dirty. To check this try testing a known good IC and see if it passes. If it fails, then clean the fingers with an alcohol (Isopropyl Alcohol) swab. Allow the fingers to dry completely before re-inserting the blade into the core module.

Follows is additiona	l information	specific to	each test.
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Test Type	Time to Complete (Approximate)	Data Displayed During Test?	Notes:
2101 5101	< 1 Second	Yes	
2016 2018	2 Seconds.	Yes	
2114 6514 9114	2 Seconds	Yes	
2125	7 Seconds	Yes	
2147	27 Seconds	Yes	
2148 2149	1 Seconds	Yes	
2465 6264	9 Seconds	Yes	
4016 6116	3 Seconds	Yes	
6810	< 1 Second	Yes	
7489	< 1 Second	Yes	*
74189	< 1 Second	Yes	
M5M5189	14 Seconds	Yes	
62256 W24257	2:02 Minutes	Yes	
W24512	2:57 Minutes	Yes	

* As of the version 2.xx code (which is also an upgraded microcontroller) the 7489 adapter board is no longer needed. If you have the need to test 7489 SRAM, you can purchase an upgraded MCU in place of the adapter board. The 7489 adapter board is no longer available.



4.0 Schematic

5.0 Card Edge to MCU / Port Expander Connections

Below is a table that lays out the pin assignment between the card edge connector, the MCU and the Port Expander.

Card	Function	Card	Function
Pin #		Pin #	
2	+5V	1	+12V
4	Ground	3	Ground
6	Card Error LED (Gnd to turn LED off)	5	Not Connected
8	ZIF Pin 1 – MCU RA0 – Q6	7	ZIF Pin 40 – +5V via Relay
10	ZIF Pin 2 – MCU RA1	9	ZIF Pin 39 – MCU RB6 or 7
12	ZIF Pin 3 – MCU RA2	11	ZIF Pin 38 – MCU RB4
14	ZIF Pin 4 – MCU RA3	13	ZIF Pin 37 – MCU RB3
16	ZIF Pin 5 – MCU RA4	15	ZIF Pin 36 – MCU RB2
18	ZIF Pin 6 – MCU RA5	17	ZIF Pin 35 – MCU RB1
20	ZIF Pin 7 – MCU RE0	19	ZIF Pin 34 – MCU RB0
22	ZIF Pin 8 – MCU RE1 – Q1	21	ZIF Pin 33 – MCU RD7
24	ZIF Pin 9 – MCU RE2 – Q2	23	ZIF Pin 32 – MCU RD6
26	ZIF Pin 10 – MCU RA7	25	ZIF Pin 31 – MCU RD5
28	ZIF Pin 11 – MCU RA6	27	ZIF Pin 30 – MCU RD4
30	ZIF Pin 12 – MCU RC0 – Q3	29	ZIF Pin 29 – MCU RC7
32	ZIF Pin 13 – MCU RC1	31	ZIF Pin 28 – MCU RC6
34	ZIF Pin 14 – MCU RC2 – Q4	33	ZIF Pin 27 – MCU RC5
36	ZIF Pin 15 – MCU RD0	35	ZIF Pin 26 – MCU RD3
38	ZIF Pin 16 – MCU RD1 – Q5	37	ZIF Pin 25 – MCU RD2
40	ZIF Pin 17 – Not Connected	39	ZIF Pin 24 – Not Connected
42	ZIF Pin 18 – Not Connected	41	ZIF Pin 23 – Not Connected
44	ZIF Pin 19 – Not Connected	43	ZIF Pin 22 – Not Connected
46	ZIF Pin 20 – Not Connected	45	ZIF Pin 21 – Not Connected
48	Switches – MCU RB5	47	I2C - SCL - MCU RC3
50	Not Connected	49	I2C - SDA – MCU RC4

6.0 SRAM Pin Assignment

	2101/	5101											
22	21	20	19	18	17	16	15	14	13	12			
VDD	A4	RW	nCS1	OD	nCS2	DO4	DI4	DO3	DI3	DO2			
A3	A2	A1	A0	A5	A6	A7	VSS	DI1	D01	DI2			
1	2	3	4	5	6	7	8	9	10	11			
	2016/	2018											
24	23	22	21	20	19	18	17	16	15	14	13		
VCC	A8	A9	nWE	nOE	A10	nCE	DQ7	DQ6	DQ5	DQ4	DQ3		
A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	GND		
1	2	3	4	5	6	7	8	9	10	11	12		
2	2114/65	14/911	4										
18	17	16	15	14	13	12	11	10					
VCC	A7	A8	A9	I/O 1	I/O 2	I/O 3	I/O 4	nW					
A6	A5	A4	A3	A0	A1	A2	nS	GND					
1	2	3	4	5	6	7	8	9					
	21	25	10			10	0						
16	15	14	13	12	11	10	9						
<u>_vcc</u>		nwe	A9	<u>A8</u>	A/	<u>A6</u>	<u>A5</u>						
nS	AU 2		A2	A3	A4	Q	v55						
1	Z	3	4	3	0	/	8						
	21	47											
18	17	16	15	14	13	12	11	10					
VCC	A6	A7	A8	A9	A10	A11	Din	nCS					
A0	A12	A2	A3	A4	A5	Dout	nWE	GND					
1	2	3	4	5	6	7	8	9					
	2148												
18	2140/	2149											
10	17	2 149 16	15	14	13	12	11	10					
VCC	17 A7	/ 2149 16 A8	15 A9	14 D0	13 D1	12 D2	11 D3	10 nWE					
VCC A6	17 A7 A5	/2149 16 <u>A8</u> <u>A4</u>	15 A9 A3	14 D0 A0	13 D1 A1	12 D2 A2	11 D3 nCS	10 nWE GND					
VCC A6 1	17 A7 A5 2	/2149 16 <u>A8</u> <u>A4</u> 3	15 A9 A3 4	14 D0 A0 5	13 D1 A1 6	12 D2 A2 7	11 D3 nCS 8	10 nWE GND 9					
VCC A6 1	17 A7 A5 2	/2149 16 A8 A4 3	15 <u>A9</u> A3 4	14 D0 A0 5	13 D1 A1 6	12 D2 A2 7	11 D3 nCS 8	10 nWE GND 9					
VCC A6 1	21465/ 17 A7 A5 2 2465/ 27	/2149 16 <u>A8</u> <u>A4</u> 3 /6264	15 <u>A9</u> A3 4	14 D0 A0 5	13 D1 A1 6	12 D2 A2 7	11 D3 nCS 8	10 nWE GND 9	10	19	17	16	15
VCC A6 1 28	2146 17 A7 A5 2 2465/ 27 pWF	/2149 16 A8 A4 3 /6264 26 CS2	15 A9 A3 4 25 A8	14 D0 A0 5 24	13 D1 A1 6 23	12 D2 A2 7 22	11 D3 nCS 8 21	10 nWE GND 9 20	19	18 D6	17	16 D4	15 D2
VCC A6 1 28 VCC	17 A7 A5 2 2465/ 27 nWE	2149 16 <u>A8</u> <u>A4</u> 3 6264 <u>26</u> <u>CS2</u> <u>A7</u>	15 A9 A3 4 25 A8 A6	14 D0 A0 5 24 A9	13 D1 A1 6 23 A11	12 D2 A2 7 22 nOE	11 D3 nCS 8 21 A10	10 nWE GND 9 20 nCS1	19 D7	18 D6	17 D5	16 D4	15 D3 VSS
VCC A6 1 28 VCC NC 1	2140 17 A7 A5 2 2465 27 nWE A12 2	/2149 16 A8 A4 3 /6264 26 CS2 A7 3	15 A9 A3 4 25 A8 A6 4	14 D0 A0 5 24 A9 A5 5	13 D1 A1 6 23 A11 A4 6	12 D2 A2 7 22 nOE A3 7	11 D3 nCS 8 21 A10 A2 8	10 nWE GND 9 20 nCS1 A1 9	19 D7 A0 10	18 D6 D0 11	17 D5 D1 12	16 D4 D2 13	15 D3 VSS 14
VCC A6 1 28 VCC NC 1	17 A7 A5 2 2465/ 27 nWE A12 2	/2149 16 A8 A4 3 /6264 26 CS2 A7 3	15 A9 A3 4 25 A8 A6 4	14 D0 5 24 A9 A5 5	13 D1 A1 6 23 A11 A4 6	12 D2 A2 7 22 nOE A3 7	11 D3 nCS 8 21 A10 A2 8	10 nWE GND 9 20 nCS1 A1 9	19 D7 A0 10	18 D6 D0 11	17 D5 D1 12	16 D4 D2 13	15 D3 VSS 14
VCC A6 1 28 VCC NC 1	17 A7 A5 2 2465, 27 nWE A12 2 4016,	/2149 16 A8 A4 3 /6264 26 CS2 A7 3 /6116	15 A9 A3 4 25 A8 A6 4	14 D0 5 24 A9 A5 5	13 D1 A1 6 23 A11 A4 6	12 D2 A2 7 22 nOE A3 7	11 D3 nCS 8 21 A10 A2 8	10 nWE GND 9 20 nCS1 A1 9	19 D7 A0 10	18 D6 D0 11	17 D5 D1 12	16 D4 D2 13	15 D3 VSS 14
VCC A6 1 28 VCC NC 1 24	2146, 17 A7 A5 2 2465, 27 nWE A12 2 4016, 23	/2149 16 A8 A4 3 /6264 26 CS2 A7 3 /6116 22	15 A9 A3 4 25 A8 A6 4 21	14 D0 5 24 A9 A5 5 20	13 D1 A1 6 23 A11 A4 6	12 D2 A2 7 22 nOE A3 7 18	11 D3 nCS 8 21 A10 A2 8 17	10 nWE GND 9 20 nCS1 A1 9	19 D7 A0 10	18 D6 D0 11	17 D5 D1 12 13	16 D4 D2 13	15 D3 VSS 14
$ \frac{VCC}{A6} 1 28 VCC 1 VCC 1 24 VCC VCC 1 $	2140/ 17 A7 A5 2 2465/ 27 nWE A12 2 4016/ 23 A9	/2149 16 A8 A4 3 /6264 26 CS2 A7 3 /6116 22 A8	15 A9 A3 4 25 A8 A6 4 21 WE	14 D0 5 24 A9 A5 5 20 OE	13 D1 A1 6 23 A11 A4 6 19 A10	12 D2 A2 7 22 nOE A3 7 18 nCS	11 D3 nCS 8 21 A10 A2 8 17 D7	10 nWE GND 9 20 nCS1 A1 9 16 D6	19 D7 A0 10 15 D5	18 D6 D0 11 14 D4	17 D5 D1 12 13 D3	16 D4 D2 13	15 D3 VSS 14
$ \begin{array}{r} 10 \\ \hline VCC \\ \hline A6 \\ 1 \\ 28 \\ VCC \\ \hline NC \\ 1 \\ 24 \\ VCC \\ \overline{A7} \end{array} $	2140/ 17 A7 A5 2 2465/ 27 nWE A12 2 4016/ 23 A9 A6	/2149 16 A8 A4 3 /6264 26 CS2 A7 3 /6116 22 A8 A5	15 A9 A3 4 25 A8 A6 4 21 WE A4	14 D0 5 24 A9 A5 5 20 OE A3	13 D1 A1 6 23 A11 A4 6 19 A10 A2	12 D2 A2 7 22 nOE A3 7 18 nCS A1	11 D3 nCS 8 21 A10 A2 8 17 D7 A0	10 nWE GND 9 20 nCS1 A1 9 16 D6 D0	19 D7 A0 10 15 D5 D1	18 D6 D0 11 14 D4 D2	17 D5 D1 12 13 D3 VSS	16 D4 D2 13	15 D3 VSS 14

	68	10													
24	23	22	21	20	19	18	17	16	15	14	13				
VCC	A0	A1	A2	A3	A4	A5	A6	RW	nCS5	nCS4	CS3				
VSS	D0	D1	D2	D3	D4	D5	D6	D7	CS0	nCS1	nCS2				
1	2	3	4	5	6	7	8	9	10	11	12				
	7489 /	74189													
16	15	14	13	12	11	10	9								
VCC	A12	A2	A3	D4	nQ4	D3	NnQ3								
A0	nME	nWE	D1	nQl	D2	nQ2	VSS								
1	2	3	4	5	6	7	8								
	M5M	5189													
24	23	22	21	20	19	18	17	16	15	14	13				
VCC	A13	A12	A11	A10	A9	NC	DQ4	DQ3	DQ2	DQ1	nW				
A0	A1	A2	A3	A4	A5	A6	A7	A8	nS	nOE	GND				
1	2	3	4	5	6	7	8	9	10	11	12				
	62256/	w24257													
28	27	26	25	24	23	22	21	20	19	18	17	16	15		
VCC	nWE	A13	A8	A9	A11	nOE	A10	nCS	D7	D6	D5	D4	D3		
A14	A12	A7	A6	A5	A4	A3	A2	A1	A0	D0	D1	D2	VSS		
1	2	3	4	5	6	7	8	9	10	11	12	13	14		
	W24	512													
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
VDD	A16	CS2	nWE	A13	A8	A9	A11	nOE	A10	nCS1	D8	D7	D6	D5	D4
NC	NC	A14	A12	A7	A6	A5	A4	A3	A2	A1	A0	D1	D2	D3	VSS
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

7.0 Parts List

- 1 Printed circuit board
- 1-40 pin socket
- 1-18 pin socket
- 3 0.1uF Ceramic Capacitors
- 1 1.0 uF Electrolytic Capacitor
- 1-2.2uF capacitor
- 1 390 Ohm Resistor (Orange, White, Brown)
- 6 1K Ohm Resistor (Brown Black Red)
- 3 10K Ohm Resistor (Brown Black Orange)
- 1 2x5 rectangle green LED
- 6-2N4401 NPN transistors
- 1 Reed Relays (Polarized)
- 1 PIC16F1519 microcontroller
- 1 MCP23008 port expander

Appendix A: Revision History

Revision A (9/2015)

• Initial release of this document

Revision B (1/2016)

• Added additional information on testing ICs and correcting testing problems.

Revision C (5/2016)

- Changed version to 2.00
- Changed the microcontroller from the PIC16F1519 to the PIC16F1719.
- Processor change eliminates the need for the 7489 adapter board as the MCU has built in pull-up resistors on all ports.
- Removed the code to detect the 7489 adapter board.
- Added code to allow the LED display colors to be reversed. This will allow users that install the bi-color LED reversed to still use the tester without having to remove the LED and re-install it. This setting is accessed via the ← and → keys and "enter" will change the setting.
- Corrected typographical error on page 9 from pin 35 equaling RD1 to the correct value 35 equaling RD3.

Revision D (11/2016)

- Version changed to 3.00
- Changed the code to increase the speed of all SRAM tests.
- Added statistics ability. Each test will keep track of how many tests have been done along with the number that failed, this statistic can be zeroed out at any time.
- Added code to permit a burn-in mode for testing, via a setting the number of test conducted on an IC can be set from 1 to 255.

Revision E (2/2017)

- Version changed to 3.01
- The increased testing speed introduced has caused testing issues with AnyPin NVRAM, these issues have been fixed.